REMARKS

Amendments to the specification

Applicant has amended paragraphs [14]-[16] to correct some mistakes found during the drafting of this response to Office action. In particular, the following changes are made:

In paragraph [14], the grammatically confusing terms "turned off" and "turned on" for switch SW_{60} are changed to "closed" and "opened", respectively. No new matter is entered.

In paragraph [15], the missing reference numeral 72 is added for the OR gate 72. No new matter entered.

In paragraph [16], the grammatically confusing terms "switched off" and "switched on" are replaced with "closed (or switched on)" and "opened (or switched off)", respectively. Additionally, the order is reversed to match "pressed or released" at the beginning of the same sentence. Also, the missing word "other" is added for the phrase "on the other hand", the mistaken word "pressed" is changed to "released" (as shown at time t3 (or t4) of figure 3), and the word "either" is moved in position to be grammatically correct. No new matter is entered.

Claim 1 is rejected under 35 USC 103a as being unpatentable over Kerr (International Publication No. WO 99/62180, hereinafter Kerr) in view of Schnizlein (US Patent No. 4,414,538, hereinafter Schnizlein).

Applicant has amended claim to state "an output end being selectively connected to one of a first voltage and a second voltage" and "generating a control signal whenever the output end of the key cell becomes to connect to the other of the second voltage and the first voltage". No new matter is entered. Applicant asserts that currently amended claim 1 should not be found unpatentable over Kerr in view of Schnizlein because there is no motivation to combine the teachings of Schnizlein with the circuit of Kerr in order to result in the present invention. Additionally, even if combined, the resulting combination does not include all the

features as claimed in claim 1 of the present invention.

The Examiner stated (see OA dated 05/01/2006), "it would have been obvious to a person of ordinary skill in the art to modify the teachings of Kerr such that the detect circuit comprised a parallel-to-serial register and electrically connected processor, as taught / suggested by Schnizlein. The suggestion / motivation for doing so would have been to convert a parallel output signal representing a scanned key module into serial data for transmission to additional processing equipment only in response to a signal from the detect circuit representative of a key depression (Schnizlein: column 4, lines 6-9). However, applicant points out that Schnizlein teaches in col 1, lines 45-48, "The invention concerns a circuit for scanning a plurality of key switches arranged in a matrix having a plurality of row conductors and a plurality of column conductors." In contrast to this requirement, the invention of Kerr illustrates a resistor ladder network 100 in figure 2. Applicant points out that the resistor ladder network 100 of Kerr is not arranged in a matrix having a plurality of row conductors and a plurality of column conductors as required by Schnizlein. For at least this reason, applicant asserts that a person of skill in the art would not be motivated to combine the teachings of Schnizlein with that of Kerr because the teachings of Schnizlein, when viewed as a whole, are directed at key switches arranged in a matrix having a plurality of row conductors and plurality of column conductors, which are not present in the circuit of Kerr.

Additionally, applicant points out that the parallel to serial converter 64 described in Schnizlein is different from the parallel to serial register mentioned in the specification of the present invention, and the combination of the analog comparator 60 and the debounce and validation logic circuit 62 mentioned in Schnizlein cannot function as the detect circuit described in the present invention. Therefore, even if combined, the combination of Schnizlein with Kerr would not result in the present invention as claimed in claim 1. In particular, the limitation "a detect circuit electrically connected to the output end of the key cell for generating a control signal whenever the voltage on the output end of the key cell becomes the second voltage or the first voltage" would not be present.

For at least the above reasons, applicant therefore asserts that currently amended claim 1 should not be found unpatentable over Kerr in view of Schnizlein because there is no motivation to combine the teachings of Schnizlein with the circuit of Kerr in order to result in the present invention. Additionally, even if combined, the resulting combination does not include all the features as claimed in claim 1 of the present invention. Reconsideration of claim 1 is respectfully requested. As claims 2-6 are dependent on claim 1, if claim 1 is found to be allowable, so too should the dependent claims 2-6.

Claims 2-4 and 6 are rejected under 35 USC 103a as being unpatentable over Kerr in view of Schnizlein as applied to claim 1 above, and further in view of Hackmeister (US Patent No. 4,027,306, hereinafter Hackmeister).

Claims 2-4 are amended to state the "one capacitor corresponding to and electrically connected to the at least one key cell within the key module", "amplifying circuit electrically connected to the capacitor", and "set of comparators electrically connected to the amplifying circuit", respectively. No new matter is entered. As mentioned above, claims 2-4 and 6 are dependent on claim 1, which is believed by applicant to be allowable over the references of Kerr and Schnizlein. Therefore, dependent claims 2-4 and 6 should also be found allowable over the cited references of Kerr and Schnizlein for at least the same reasons as provided for claim 1 above. Reconsideration of claims 2-4 and 6 is respectfully requested.

Claim 5 is rejected under 35 USC 103a as being unpatentable over Kerr, Schnizlein and Hackmeister as applied to claims 1-4 and 6 above, and further in view of Johnson (US Patent No. 6,265,993 B1, hereinafter Johnson).

As mentioned above, claim 5 is dependent on claim 1, which is believed by applicant to be allowable over the references of Kerr and Schnizlein. Therefore, claim 5 should also be found allowable over the cited references of Kerr and Schnizlein for at least the same reasons as provided for claim 1 above. Reconsideration of claim 5 is respectfully requested.

Claim 5 is rejected under 35 USC 103a as being unpatentable over Kerr, Schnizlein and Hackmeister as applied to claims 1-4 and 6 above, and further in view of Figie et al. (US Patent No. 5,872,561 B1, hereinafter Figie).

As mentioned above, claim 5 is dependent on claim 1, which is believed by applicant to be allowable over the references of Kerr and Schnizlein. Therefore, claim 5 should also be found allowable over the cited references of Kerr and Schnizlein for at least the same reasons as provided for claim 1 above. Reconsideration of claim 5 is respectfully requested.

New Claims 7-15

Applicant has added new claims 7-15. The difference between claim 1 and claim 7 is that in claim 7 the detect circuit is detecting a transient voltage at the moment when the key cell is pressed or released and then generating a control signal. And the processor is for controlling the parallel-to-serial register only upon reception of the control signal. No new matter is entered. In particular, the above claimed operation of the detect circuit is shown in Fig.3 and described in paragraphs [12] to [16], and the above claimed operation of the processor is described in paragraphs [12], [17], and paragraph [18].

Concerning the patentability of claim 7 over the cited references of Kerr and Schnizlein, applicant points out that neither Kerr nor Schnizlein teach a detect circuit for asserting a control signal both upon detecting a transient voltage at the moment when the key cell is pressed or released. That is, both Kerr and Schnizlein simply watch for key presses but not look for when a key is released. Applicant points out col 4, lines 6-19 of Schnizlein stating, "the parallel to serial converter 64 accepts the ROM decoder 66 output only in the response to a signal from the debounce and validation logic unit 62 in response to an activated keyswitch signal on line 65" (emphasis added) Also of note is that Kerr teaches on page 7, lines 12-14, "In summary, comparison circuit 206 functions to allow only certain predetermined switch closures, or combination of switch closures, to generate an interrupt signal to decoder 212." For at least these differences, applicant asserts that claim 7 should be found allowable over the cited references Kerr and Schnizlein. Consideration of newly added

claim 7 is respectfully requested. As claims 8-15 are dependent on claim 7, if claim 7 is found allowable, so too should dependent claims 8-15.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)